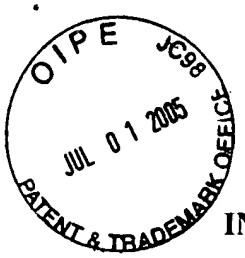


IFW

PATENT
P57012

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Application of:

Hoon KIM

Serial No.: 10/798,574 Examiner: Thomas L. Dickey

Filed: 12 March 2004 Art Unit: *2826*

For: THIN FILM TRANSISTOR AND METHOD FOR FABRICATING THE SAME.

## INFORMATION DISCLOSURE STATEMENT

**Mail Stop: Application Number**
Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with 37 C.F.R. §1.56, and §§1.97 and 1.98 as amended, Applicant cites and describes the following art references.

In accordance with the new regulation set forth in the Official Gazette Notices: 05 August 2003 (a copy attached herewith), a copy of the U.S. patent references cited below is not attached.

### OTHER DOCUMENT

- United States Patent No.5,492,843 to Hiroki Adachi, et al., entitled, *METHOD OF FABRICATING SEMICONDUCTOR DEVICE AND METHOD OF PROCESSING SUBSTRATE,* issued on 20 February 1996.

Folio: P57012

Date: 7/1/05

I.D.: REB/cg

## DISCUSSION

**Adachi, et al., 843** discloses the "Method of fabricating a semiconductor device. A glass substrate such as Corning 7059 is used as a substrate. A bottom film is formed. Then, the substrate is annealed above the strain point of the glass substrate. The substrate is then slowly cooled below the strain point. Thereafter, a silicon film is formed, and a TFT is formed. The aforementioned anneal and slow cooling reduce shrinkage of the substrate created in later thermal treatment steps. This makes it easy to perform mask alignments. Furthermore, defects due to misalignment of masks are reduced, and the production yield is enhanced. In another method, a glass substrate made of Corning 7059 is also used as a substrate. The substrate is annealed above the strain point. Then, the substrate is rapidly cooled below the strain point. Thereafter, a bottom film is formed, and a TFT is fabricated. The aforementioned anneal and slow cooling reduce shrinkage of the substrate created in later thermal treatment steps. Thus, less cracks are created in the active layer of the TFT and in the bottom film. This improves the production yield. During heating of the substrate, it is held substantially horizontal to reduce warpage, distortions, and waviness of the substrate."

The citation of the foregoing references is not intended to constitute an assertion that other or more relevant art does not exist. Accordingly, the Examiner is requested to make a wide-ranging and thorough search of the relevant art.

Pursuant to 37 CFR § 1.97(d), the undersigned attorney hereby certifies that each item of information contained in this Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign patent application not more than three(3) months prior to the filing of the statement.

No fee is incurred by this Statement.

Respectfully submitted,

Robert E. Bushnell
Reg. No.: 27,774

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Folio: P57012
Date: 1 July 2005
I.D.: REB/cg

| INFORMATION DISCLOSURE STATEMENT<br>PTO-1449 (PAGE 1 OF 1) | SERIAL NUMBER 10/798,574 | DOCKET NO. P57012 |
|---|---|---|
| | APPLICANT Hoon KIM | |
| | FILING DATE 12 March 2004 | GROUP |



**U.S. PATENT DOCUMENTS**

| EXAMINER | DOCUMENT NUMBER | DATE | NAME | CLASS | SUBCLASS | FILING DATE |
|---|---|---|---|---|---|---|
| | 5,492,843 | 2/20/96 | Adachi, et al. | | | 29 July 1994 |
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**FOREIGN PATENT DOCUMENTS**

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|---|---|---|---|---|---|---|---|
| | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUBCLASS | YES | NO |
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**OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)**

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| *EXAMINER:* | *DATE CONSIDERED:* |
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP §609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.*

# United States Patent and Trademark Office OG Notices: 05 August 2003

Information Disclosure Statements
May Be Filed Without Copies of
U.S. Patents and Published Applications in
Patent Applications filed after June 30, 2003

Background

The U.S. Patent and Trademark Office (USPTO or Office) regulations concerning Information Disclosure Statements (IDSs) currently require that copies of the cited references be submitted with the IDS listing. See 37 CFR 1.98 (a)(2). In a prior notice in the Official Gazette this requirement was partially waived with respect to U.S. patents and U.S. patent application publications when an applicant submitted an IDS using the Office's electronic filing system (as an electronic IDS, eIDS). See Legal Framework for the Use of the Electronic Filing System, 1263 Off. Gaz. Pat. Off. 60, 10/8/2002, Part V.

All U.S. applications1 filed after June 30, 2003 are stored in electronic form in the Office's Image File Wrapper (IFW) system.2 IDSs submitted for these electronic applications are processed by Office staff to create an electronic link which permits cited U.S. patents and U.S. patent application publications to be conveniently viewed by examiners through the Office's patent search system. This feature enables the Office to avoid scanning these documents into IFW, obviating the need for their submission.

Waiver

The Office hereby waives the requirement under 37 CFR 1.98 (a)(2)(i) for submitting a copy of each cited U.S. patent and each U.S. patent application publication for all U.S. national patent applications filed after June 30, 2003 and for all international applications that have entered the national stage under 35 USC 371 after June 30, 2003. See 37 CFR 1.491(b). For all patent applications filed on or before June 30, 2003, copies of cited U.S. patents and patent application publications are still required unless an eIDS is filed.

Applicants are still required to submit copies of foreign patent documents and non-patent literature in accordance with 37 CFR 1.98(a)(2).

FOR FURTHER INFORMATION CONTACT:

Questions concerning this waiver may be submitted to Jay Lucas by e-mail at Jay.Lucas@uspto.gov or by telephone at (703) 308-6868. Comments may also be submitted by mail addressed to: Commissioner for Patents, Box Comments - Patents, Post Office Box 1450, Alexandria, VA 22313-1450, or by facsimile to (703) 305-2919, marked to the attention of Jay Lucas.

STEPHEN G. KUNIN
Deputy Commissioner for
Patent Examination Policy

1 Except in special situations, such as in applications under secrecy order or containing national security markings.

2 See Notification of United States Patent and Trademark Office Patent Application Records being Stored and Processed in Electronic Form, 1271 Off. Gaz. Pat. Off. 100, 6/17 2003.